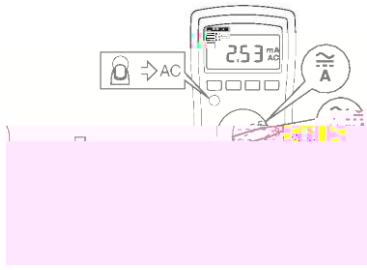
2018.08


AC
2.53
A


SINE
TH-SG10 型数字合成信号发生器


RIGOL
DS 5062C

1

2

3 Q Av Ri R0

4

1

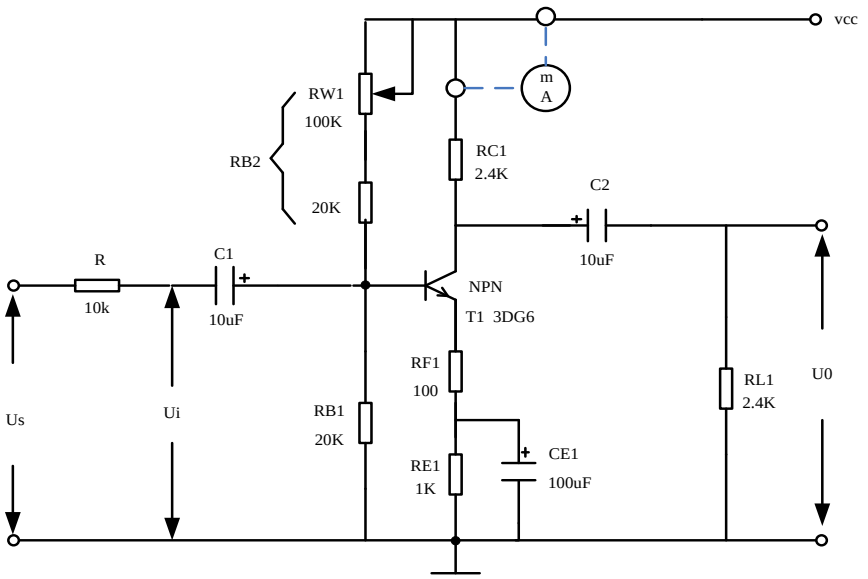
2

3

1

2

1 , 2-1



2-1

2

a)

b)

+12V U_i U_s

R_{W1} $V_E = 2.2V$ V_{BE} V_{CE} R_{B2}

2.1

2.1

V_{BEQ} V	V_{CEQ} V	R_{B2} K

c) R_{W1} $V_E = 2.2V$ I_C

T1 V_B R_{B2} R_{B1}

2.2 T1 I_B β

$$I_B = \frac{V_{CC} - V_B}{R_{B2}} - \frac{V_B}{R_{B1}} \qquad \beta = \frac{I_C}{I_B}$$

I_B

2.2 I_B β

2.2

I_C (mA)	V_B (V)	R_{B2} ($K\Omega$)	R_{B1} ($K\Omega$)	I_B (mA)	β

3

1 f=1KHZ 50mV

U_i U_i U_0

U_i U_0 2.3

(2) U_i f=1KHZ U_i

U_0 U_0 2.3

2.3

Ui(mV)	U_O(V)	Av	Av
50mV_{P-P}			

U_i U_0

2.3 V_{P-P}

V_{RMS}

(3) Ui=50 mV f=1kHz R_{L1} R_{L1}

2.4

2.4

R_{C1}	R_{L1}	Ui(mV)/ V_{P-P}	U_O(V)/ V_{P-P}	Av	Av
2.4k	2.4K	50mV_{P-P}			
2.4k	10K	50mV_{P-P}			

(4) Ui=50 mV f=1kHz R_{W1} U_O

U_B U_C U_E 2.5

2.5

R_{W1}	U_B(V)	U_C(V)	U_E(V)	U_O

U_i

1

2

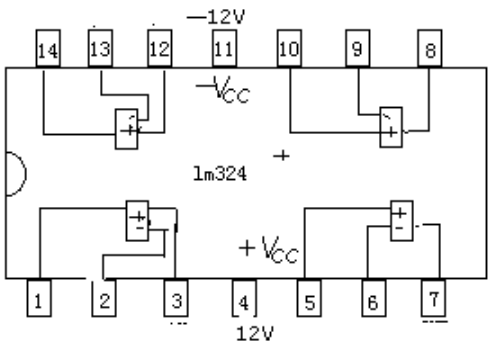
3

V_O A_f

V_O

4-1

4.1



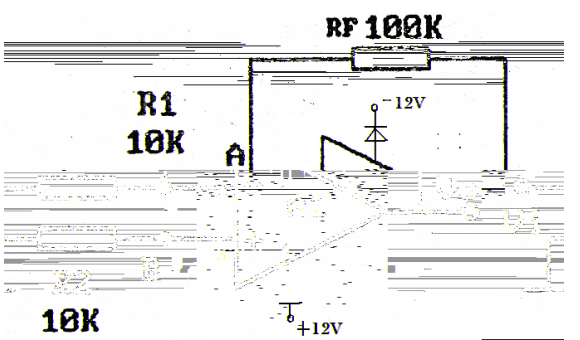
LM324

4-1

Vi V		0	0.5	1	1.5	2
Vo(V)	R_L=					
	R_L=10K					

2

4-2

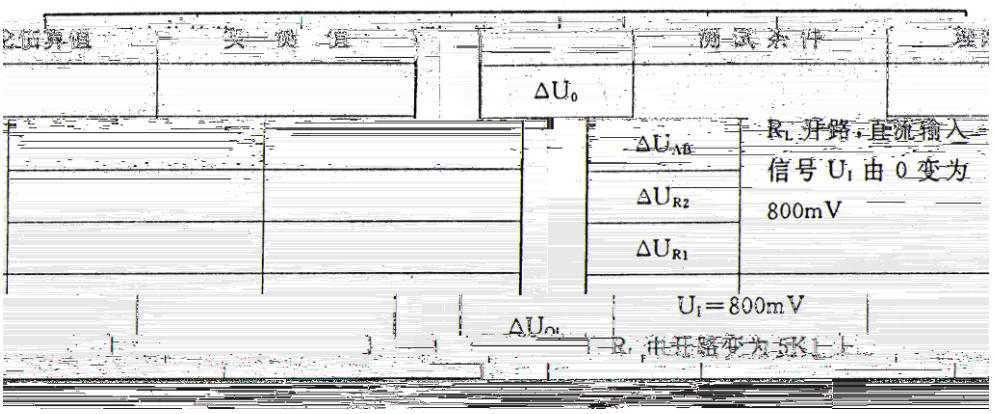


4-2

4-2 4-2

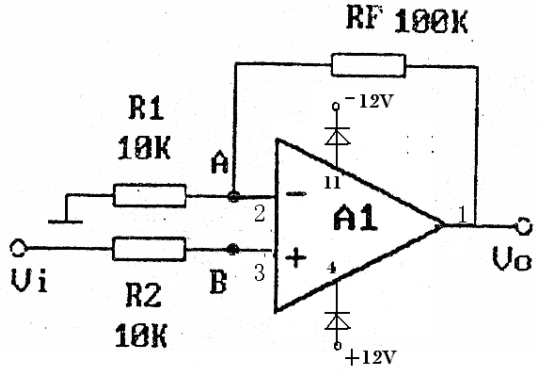
4-2

4-3 4-3



3

4.3 4-4 4-5 4-4 4-5



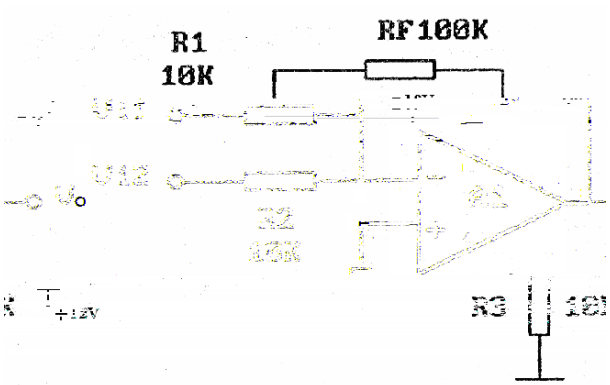
4-3

4-5

	测 试 条 件	理论估算值	实 测 值
ΔU_o	R_L 开路，直流输入信号 U_I 由 0 变为 800mV		
ΔU_{AB}			
ΔU_{R2}			
ΔU_{R1}			
ΔU_{OL}	U_I=800mV		

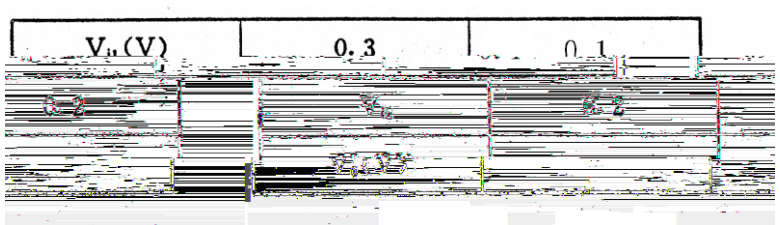
4

4-4



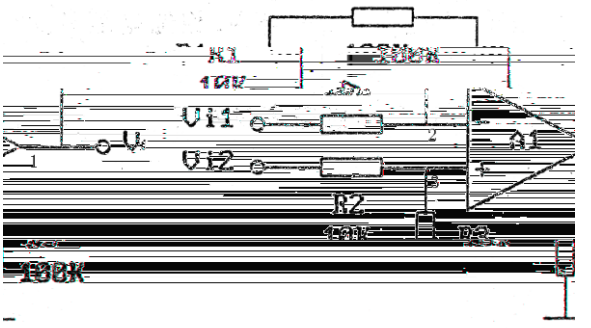
4.4

4-6



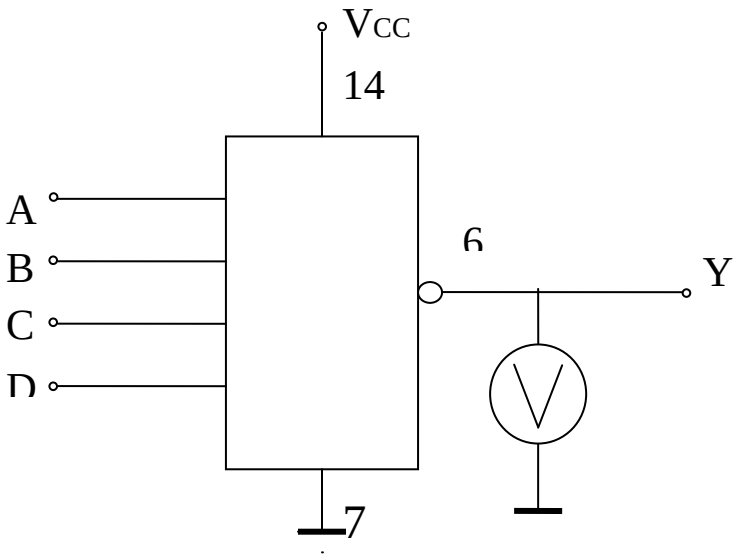
5

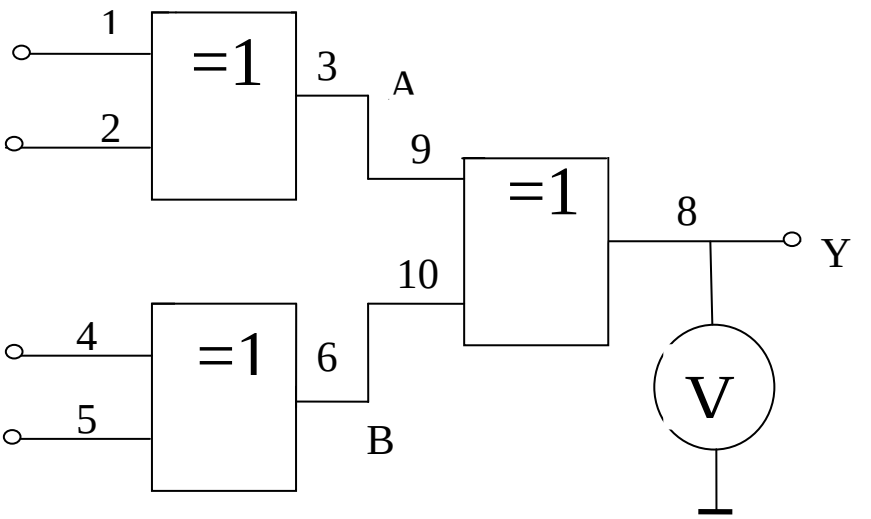
4.5 4.7

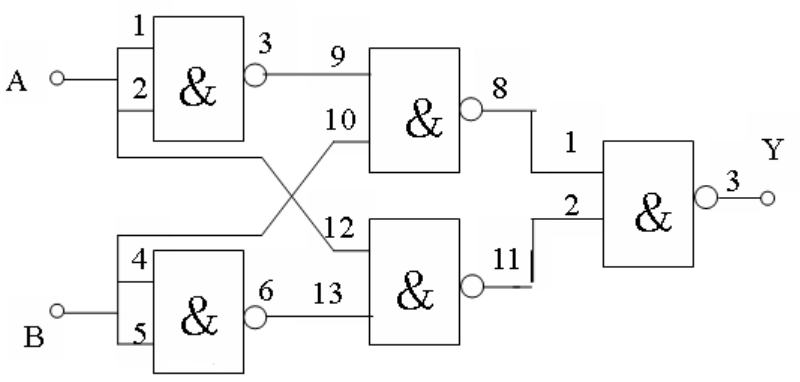


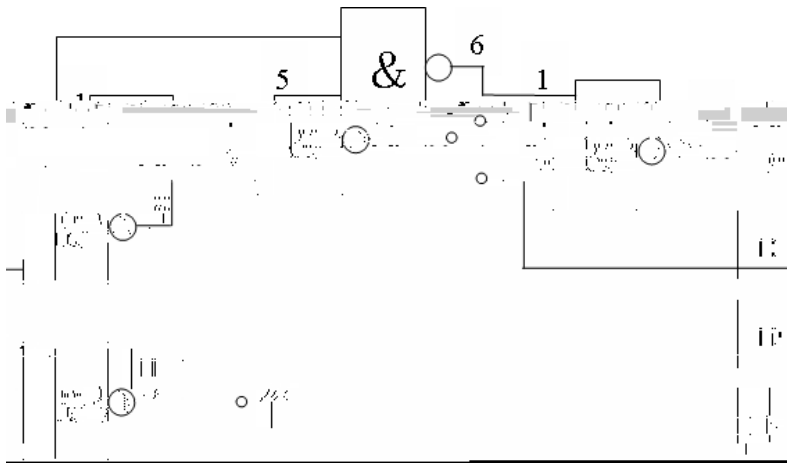
4.5

V_{i1}(V)	1	2
V_{i2}(V)	0.5	1.8
V_o(V)		


VCC
14
A
B
C
D
6
Y
7


1
=1
3
A
2
9
=1
8
Y
10
4
=1
6
V
5
B

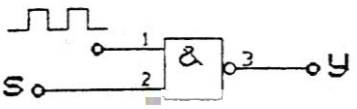

A
B
Y
1
2
3
4
5
6
8
9
10
11
12
13
&


5
6
1
&

$$F = \overline{\overline{A + B}} = \overline{\overline{A} \bullet \overline{B}}$$

5. 利用与非门控制输出。

用一片 74LS00 按图 1.6 接线，S 接任一电平开关，用示波器观察 S 对输出脉冲的控制作用。



一、实验目的

1. 掌握组合逻辑电路的功能测试。
2. 验证半加器和全加器的逻辑功能。
3. 学会二进制数的运算规律。

二、实验仪器及材料

器件

3 片	74LS00　二输入端四与非门
1 片	74LS86　二输入端四异或门
1 片	74LS54　四组输入与或非门

三、预习要求

1. 预习组合逻辑电路的分析方法。
2. 预习用与非门和异或门构成的半加器、全加器的工作原理。
3. 预习二进制数的运算。

四、实验内容

1. 组合逻辑电路功能测试。

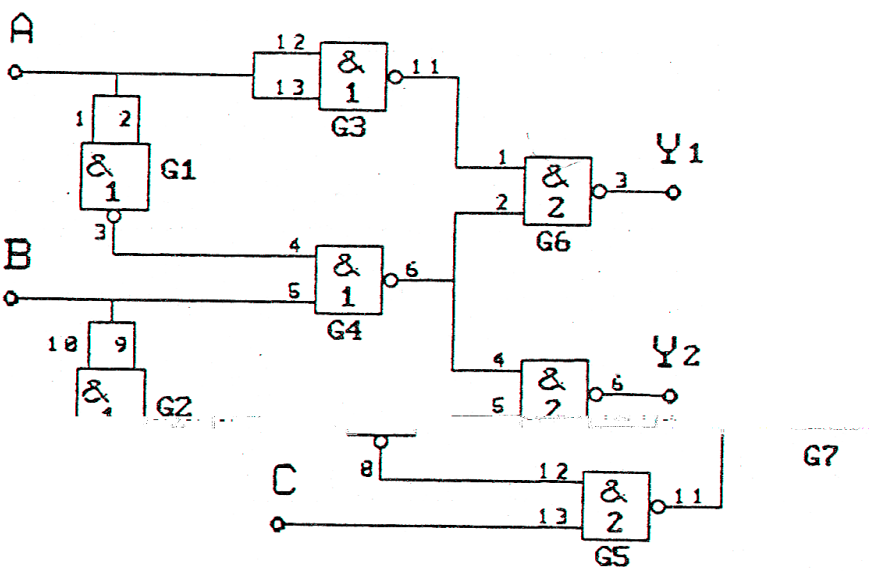


图 6.1

(1). 用 2 片 74LS00 组成图 6.1 所示逻辑电路，为便于接线和检查，在图中要注明芯片

编号及各引脚对应的编号。

(2). 图中 A、B、C 接电平开关，Y1、Y2 接发光管电平显示。

(3). 按表 6.1 要求，改变 A、B、C 的状态填表并写出 Y1、Y2 逻辑表达式。

(4). 将运算结果与实验比较。

表6.1

输入			输出	
A	B	C	Y_1	Y_2
0	0	0	0	0
0	0	1	0	1
0	1	0	1	1
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

2. 测试用异或门(74LS86)和与非门组成的半加器的逻辑功能。

根据半加器的逻辑表达式可知，半加器 Y 是 A、B 的异或，而进位 Z 是 A、B 相与，因此可用一个异或门和一个与门组成如图 6.2 的电路。

表6.2

输入端	A	0	1	0	1
	B	0	0	1	1
输出端	Y				
	Z				

3. 测试用异或、与或非和非门组成的全加器的逻辑功能

[illegible]中，常用一块双异或门[illegible]全加器可以用两个半加器和两个与门一个或门组成，在实[illegible]

[illegible]个异或非门和[illegible]个与非门实现。

电路图，写出逻辑表达式。

[illegible]线，接线时注意与或非门[illegible]

(1). 画出用异或门、与或非门和非门实现全加器的逻辑电[illegible]

(2). 找出异或门、与或非门和与门器件按自己画出的图[illegible]

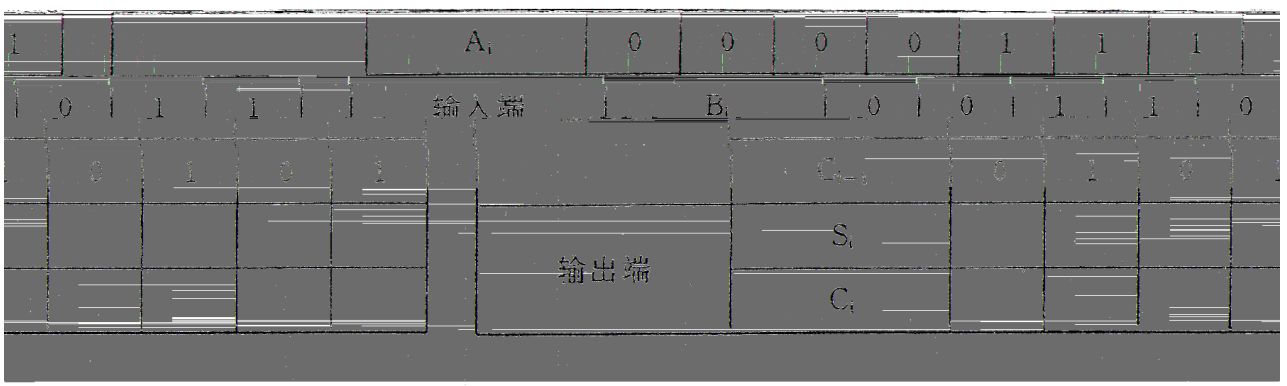
不用的与门输入端接地。

用表测量 S_i 和 C_i 的电位并将其转为逻

(3). 当输入端 A_i、B_i 及 C_{i-1} 为下列情况时，用万辑状态填入下表。

表6-3

B_i	C_{i-1}	C_i	S_i	A_i	
0	0			0	
1	0			0	
	0	0			1
	1	0			1
	0	1			0
	1	1			0
1	0	1			
1	1	1			



五、实验报告

[illegible]整理实验数据，图表并对实验结果进行分析讨论

法。

2. 总结组合逻辑电路的分析方

1 555

2

3

4

5

1

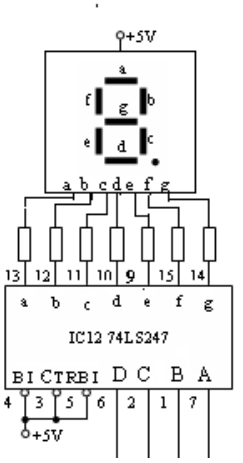
2

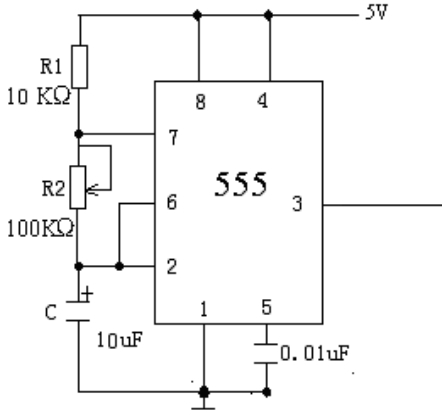
3

2. 160 7-2 2

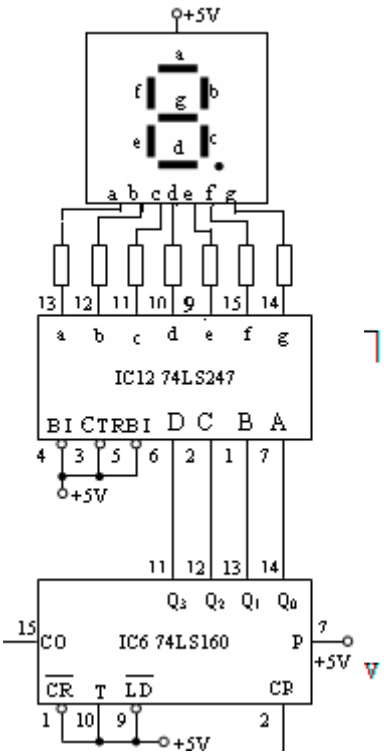
7-1

D	C	B	A	
0	0	0	0	
0	0	0	1	
0	0	1	1	
0	1	0	1	
0	1	1	1	
1	0	0	1	

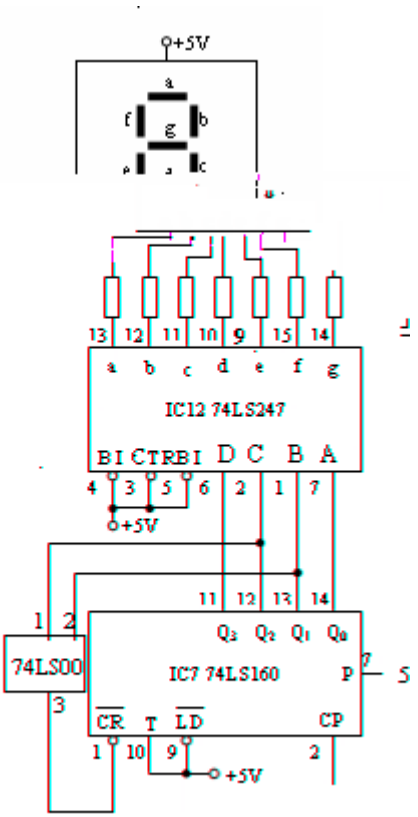




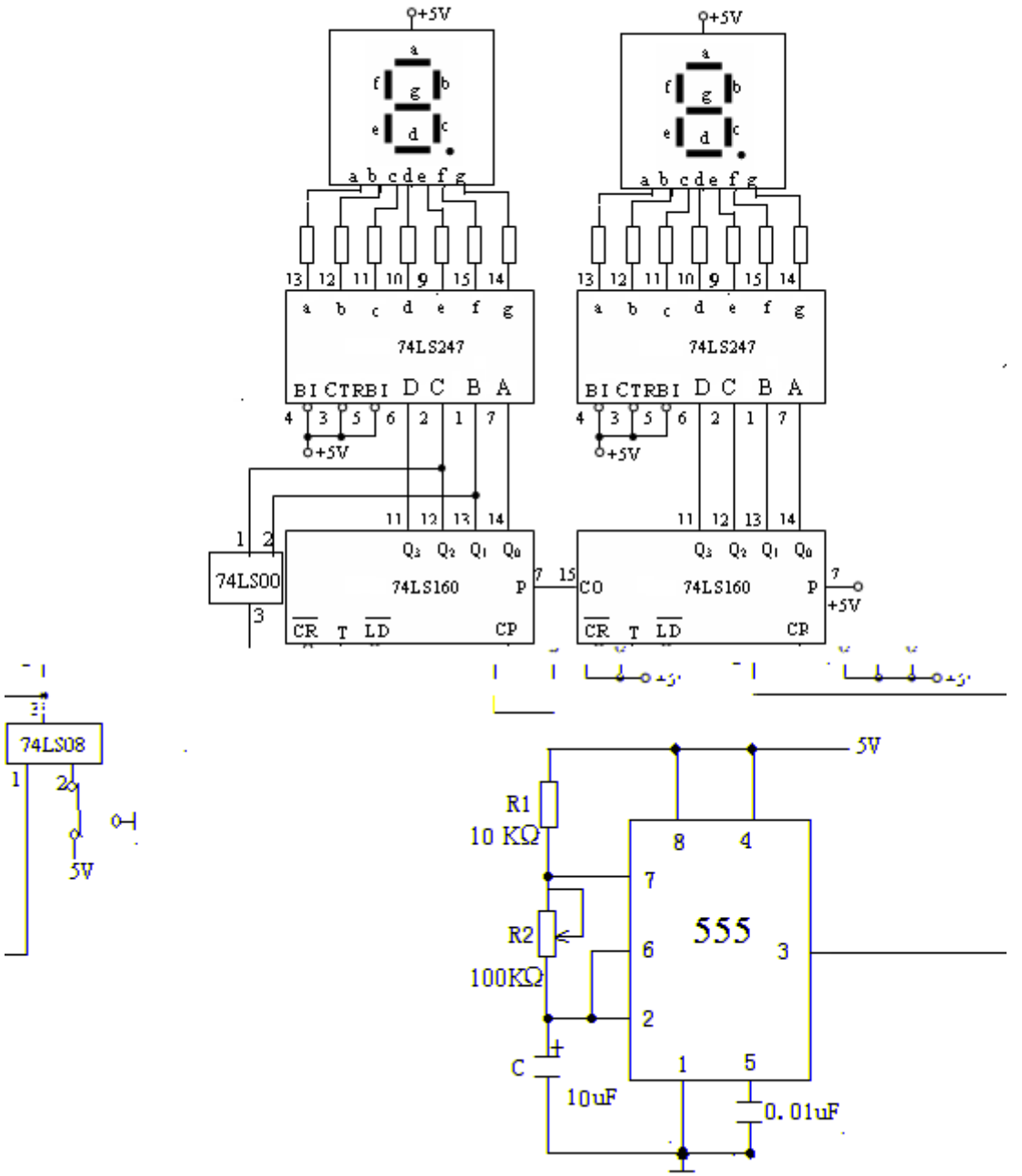
7-4

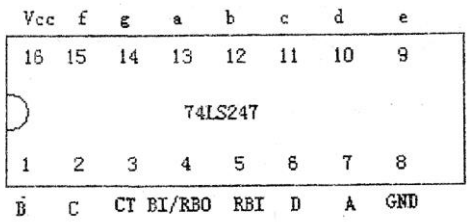

+5V
a
f
g
b
e
d
c
a b c d e f g
13 12 11 10 9 15 14
a b c d e f g
IC12 74LS247
BI CTRBI D C B A
4 3 5 6 2 1 7
+5V
11 12 13 14
Q3 Q2 Q1 Q0
15
CO
IC6 74LS160
P
7
+5V
CR T LD
CP
1 10 9
2
+5V

7-2

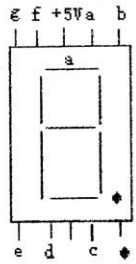

+5V
a
f
g
b
13 12 11 10 9 15 14
a b c d e f g
IC12 74LS247
BI CTRBI D C B A
4 3 5 6 2 1 7
+5V
11 12 13 14
1 2
Q3 Q2 Q1 Q0
74LS00
IC7 74LS160
P
7
3
CR T LD
CP
1 10 9
2
+5V

7-3


+5V
a
b
c
d
e
f
g
a b c d e f g
13 12 11 10 9 15 14
74LS247
BI CTRBI D C B A
4 3 5 6 2 1 7
11 12 13 14
Q3 Q2 Q1 Q0
74LS160
P
CO
CR T LD
CP
74LS00
74LS08
1 2 3
5V
R1
10 KΩ
R2
100KΩ
C
10uF
555
8 4 7 6 3 2 1 5
0.01uF



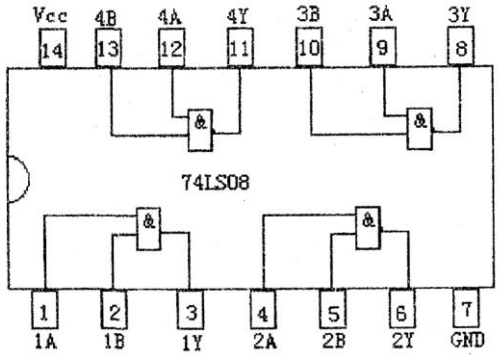
74LS247 管脚图

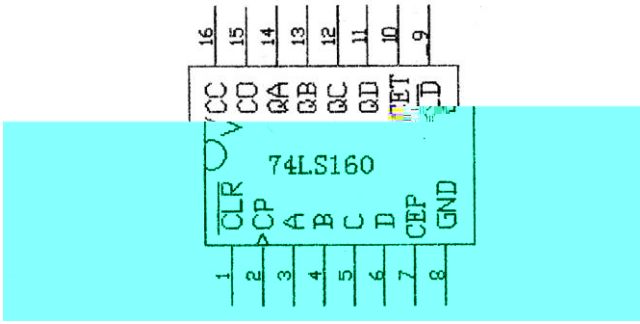


数码管脚图

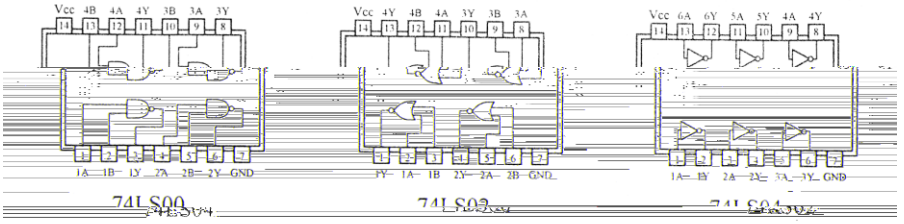
74LS247 功能表:

CT	RBI	BI/RBO	D C B A	a b c d e f g	显示
0	×	1	× × × ×	0 0 0 0 0 0 0	测试
×	×	0	× × × ×	1 1 1 1 1 1 1	全灭
1	1	1	0 0 0 0	0 0 0 0 0 0 1	0
1	1	1	1 0 0 1	0 0 0 0 1 0 0	9

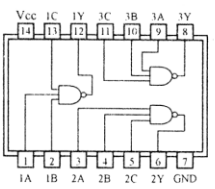




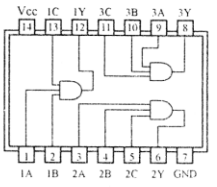
74LS08　　74LS160



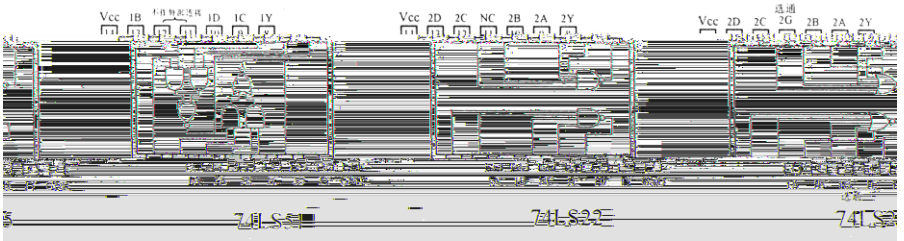
74LS20



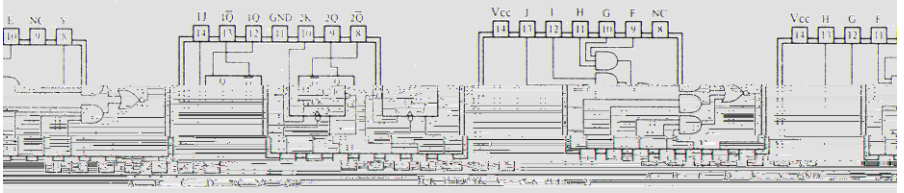
74LS10



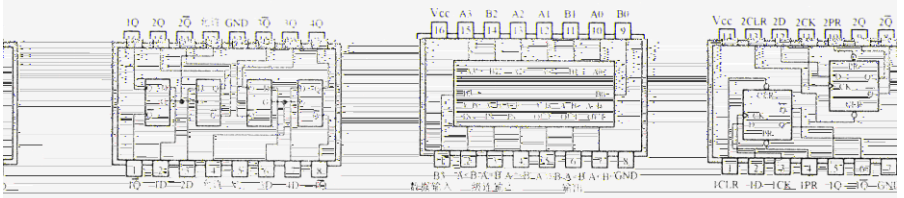
74LS11



74LS55



74LS73

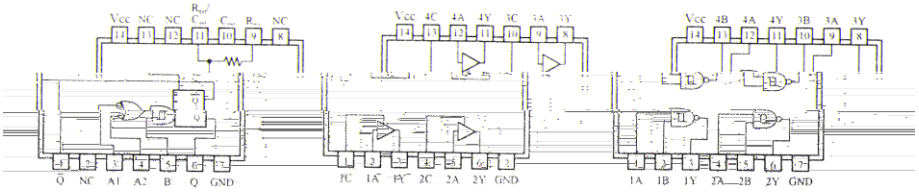


74LS75

74LS85

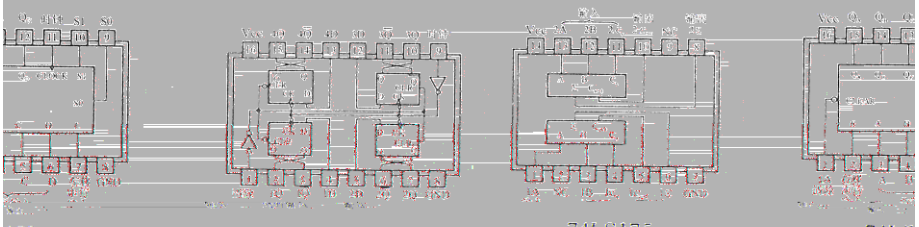
74LS74

74LS86 74LS90 74LS112

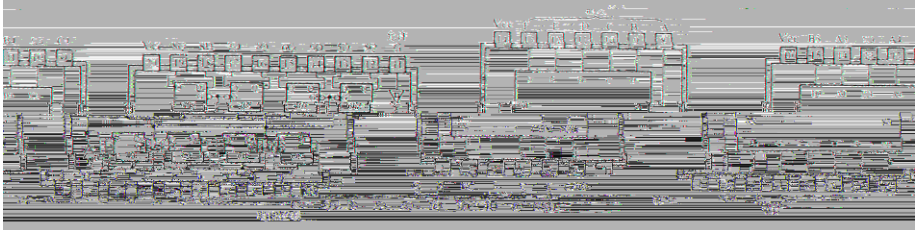


74LS121 74LS126 74LS132

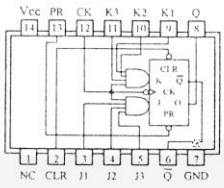
74LS161 74LS139 74LS153 74LS160



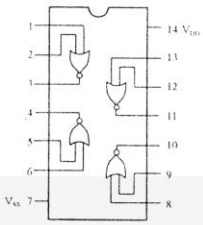
183 74LS194 74LS175 74LS



74LS283 74LS373 74LS280



74H72



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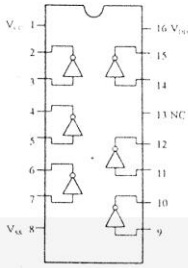

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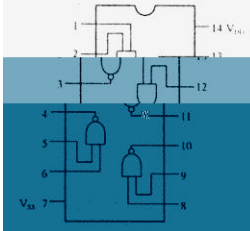

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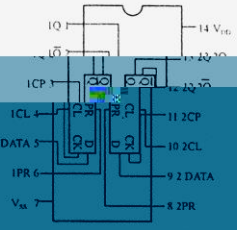

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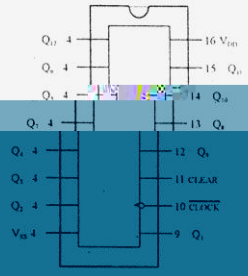

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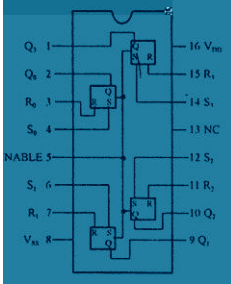

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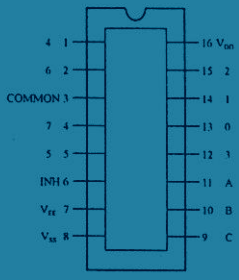

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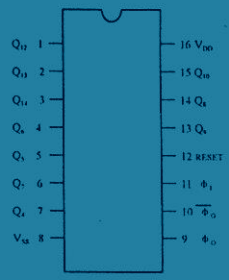

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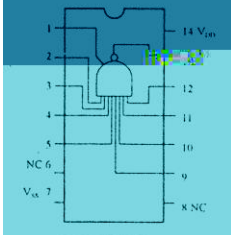

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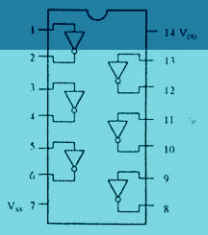

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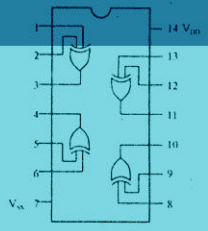

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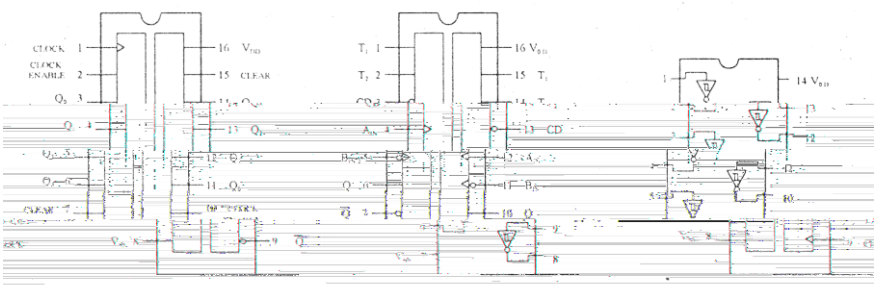

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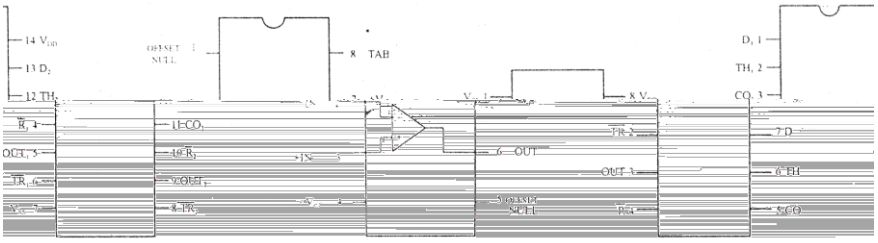

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